

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kerry Bernstein, et al.

Examiner: Unassigned

Serial No: 10/604179

Art Unit: Unassigned

Filed:

4/30/03

Docket: BUR920010207US1 (15821)

For: METHODOLOGY FOR FIXING Qcrit

**Dated:** June 16, 2003

AT DESIGN TIMING IMPACT

Commissioner for Patents United States Patent and Trademark Office Alexandria, Virginia 22313-3513

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Chan, "Technique for Reducing Personalized Array Soft Errors', RESEARCH DISCLOSURE, Kenneth Mason Publications Ltd, England, October 1989, No. 306;

## CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

Dated: 7-14-03

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- 2. Jarvela, et al., "MLC DESIGN TO LIMIT SOFT ERROR FAILS", <u>IBM</u> <u>Technical Disclosure Bulletin</u>, Vol. 27, No. 2, July 1984, pp. 1343-1344;
- 3. Geppert, et al., "CMOS DRAM DESIGN LAYOUT TO IMPROVE SOFT ERROR IMMUNITY", <u>IBM Technical Disclosure Bulletin</u>, Vol. 34, No. 4B, September 1991, pp. 277-28; and
- 4. Dai, et al., "Alpha-SER Modeling & Simulation for Sub-0.25μm CMOS Technology", 1999 Symposium on VLSI Technology Disgest of Technical Papers, pp. 81-82.

Applicants are submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. §1.97(b), no petition, certification or fee is required.

Respectfully submitted,

John & Benony John S. Sensny

Registration No. 28,757

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